**[Programmable Communication Group](https://sites.google.com/a/temple.edu/programmable-communication-group/)**

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| Date | Friday, November 08, 2013 | | |
| Advisor | Dr. Silage | | |
| Members | Cedric Destin | Brandon Keith | Brian Thibodeau |

Headline: It is crunch time! Keep in mind that the Preliminary Prototype is due 11/22 and the Design Document is due 12/02.

Topics to discuss (with Silage)

* Provide updated design document draft with updated sections 1.1 (Overall objective) and 1.2 (Historical and Economic Perspective).
* Analytical expressions for PLL?

Topics to discuss (among SD team and Silage, if necessary)

* Scheduling/tasking for the remainder of SD1.

Dr. Silage feedback

Topics to discuss in next SD meeting

* Provide updated design document draft with updated sections 1.3-1.5.

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| **Engineer** | **Status** |
| Brian Thibodeau | * Squaring Loop and Costas Loop used for BPSK demodulation are complete and working, but the analytical analysis describing loop behavior doesn’t match simulation results. * According to the *Synchronization* chapter in the Digi. Comm. Book, linear analysis of PLL’s is only performed when the loop is tracking. During acquisition, non-linear analysis must be applied. * As a result of this find, Phase-plane analysis is being used to explore stability regions during acquisition. This is being done using ODE solver. The ODE solver also provides the state response for the phase error * Also recognized that the 2fc filter used in the phase detector is NOT filtering out the double frequency component. This is the focus of current efforts to reconcile the analytical analysis with simulation results. |
| Cedric Destin | * Implementing BFSK demodulation using PLL * Implemented BFSK demodulation using optimal non-coherent receiver |
| Brandon Keith | * Updating sections 1.3 – 1.5 of DD draft * Researching FEC methods * Researching interleaving methods |